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CS5106

Multi-Feature, Synchronous plus Auxiliary PWM Controller

Description

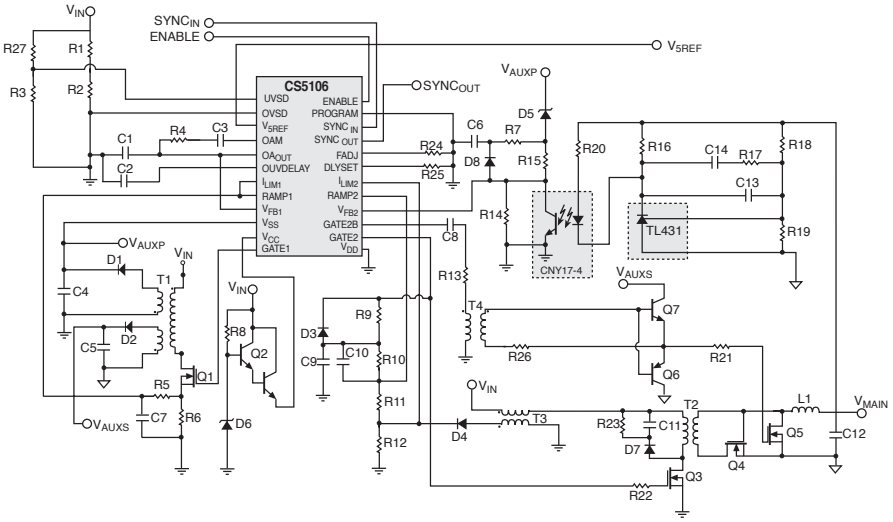
The CS5106 is a fixed frequency, current mode controller with one single NFET driver and one dual FET, synchronous driver. The synchronous driver allows for increased efficiency of the main isolated power stage and the single driver allows the designer to develop auxiliary supplies for controller power as well as secondary side house keeping. In addition, because the synchronous drivers have programmable FET non-overlap, the CS5106 is an ideal controller for soft-switched converter topologies.

The CS5106 is specifically designed for isolated topologies where speed, flexibility, reduced size and reduced component count are requirements. The controller contains the following features: Undervoltage Shutdown, Overvoltage Shutdown, Programmable Frequency, Programmable Synchronous Non-Overlap Time, Master/Slave Clocking with Frequency Range Detection, Enable, Output Undervoltage Protection with Timer, 20mA 5V Output, 80ns PWM propagation delay, and Controlled Hiccup Mode.

The CS5106 has junction temperature and supply ranges of -40˚C to 125˚C and 9V to 16V respectively and is available in the 24 lead SSOP package.

Applications Diagram

48V to 3.3V Forward Converter with Synchronous Rectifiers

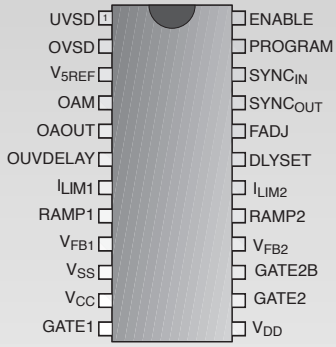


Features

- Programmable Fixed Frequency
- Programmable FET Non-overlap
- Enable Lead
- 12V Fixed Auxiliary Supply Control
- Under and Overvoltage Shutdown
- Output Undervoltage Protection with Timer
- Master/Slave Clock Syncing Capability
- Sync Frequency Range Detection
- 80ns PWM Propagation Delay
- 20mA 5V Reference Output
- Small 24 lead SSOP Package
- Controlled Hiccup Mode

Package Options

24 Lead SSOP



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Absolute Maximum Ratings

Operating Junction Temperature, T_J ..... 150°C
Operating Temperature Range, T_A .....-40 to 85°C
Storage Temperature Range, T_S.....-65 to 150°C
ESD (Human Body Model).....2kV
Lead Temperature Soldering: Reflow (SMD styles only).....60 sec. max above 183°C, 230°C peak

Lead Symbol	Lead Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
UVSD	Undervoltage Shutdown Input	6V	-0.3V	1mA	N/A
OVSD	Overvoltage Shutdown Input	6V	-0.3V	1mA	N/A
V_{5REF}	5V Reference Output	6V	-0.3V	150mA	25mA
OAM	Error Amp Minus Input	6V	-0.3V	250µA	1.2mA
OAOUT	Error Amp Output	6V	-0.3V	300µA	100mA
OUVDELAY	Output Overcurrent Timer Capacitor	6V	-0.3V	15µA	N/A
I_{LIM1}	Auxiliary Primary Side Current Limit Input	6V	-0.3V	10µA	N/A
RAMP1	Auxiliary Primary Side Current Ramp Input	6V	-0.3V	10µA	N/A
V_{FB1}	Auxiliary Voltage Feedback Input	6V	-0.3V	5µA	100µA
V_{SS}	Bootstrapped Power Input	20V	-0.3V	2µA	0.5A Peak 300mA DC
V_{CC}	Main Power Input	20V	-0.3V	See Note 1	0.5A Peak 300mA DC
GATE1	Auxiliary FET Driver Output	20V	-0.3V	0.5A Peak 100mA DC	0.5Peak 100mA DC
Gnd	Ground	0V	0V	0.5A Peak	N/A 300mA DC
GATE2	Synchronous FET Driver Output	20V	-0.3V	0.5A Peak 100mA DC	0.5APeak 100mA DC
GATE2B	Synchronous FET Driver Output B	20V	-0.3V	0.5A Peak 100mA DC	0.5A Peak 100mA DC
V_{FB2}	Synchronous Voltage Feedback Input	6V	-0.3V	10µA	100µA
RAMP2	Synchronous Primary Side Current Ramp Input	6V	-0.3V	10µA	N/A
I_{LIM2}	Synchronous Primary Side Current Limit Input	6V	-0.3V	10µA	N/A
DLYSET	Gate Non-Overlap Programming Input	2.5V	-0.3V	125µA	N/A
FADJ	Frequency Programming Input	2.5V	-0.3V	125µA	N/A
$SYNC_{OUT}$	Clock Master Output	6V	-0.3V	50mA	100mA
$SYNC_{IN}$	Clock Slave Input	6V	-0.3V	N/A	1mA
PROGRAM	Enable Programming Input	16V	-0.3V	30µA	N/A
ENABLE	Enable Input	16V	-0.3V	300µA	N/A

Note 1: Current out of V_{CC} is not limited. Care should be taken to prevent shorting V_{CC} to Ground.

Electrical Characteristics: T_J = -40°C to 125°C, V_{SS} = 9 to 16V, V_{5REF} I_{LOAD} = 2mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD=6V, OVSD = 0V, ENABLE = 0V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3V, R_{FADJ} = R_{DLYSET} = 27.4kΩ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **V_{SS} Supply Current**	Measure current into V_{SS} when V_{5REF} I_{LOAD}=0mA. 9V ≤ V_{SS} ≤ 13V.		16.00	23.00	mA
	Measure current into V_{SS} when V_{5REF} I_{LOAD}=0mA. 13V < V_{SS} ≤ 16V.		16.00	25.00	mA
	Measure current into V_{SS} when V_{5REF} I_{LOAD}=0mA. 16V < V_{SS} ≤ 20V.		16.00	30.00	mA
■ **Low V_{CC} Supply Current**	Float V_{SS}. Set V_{CC}=7V & measure V_{CC} current while V_{5REF} I_{LOAD}=0mA.		1.50	3.50	mA
■ **V_{SS} TO V_{CC} DIODE**					
Diode ON Voltage	Measure V_{SS} - V_{CC}.	0.20	0.75	1.00	V
■ **Reference**					
5V Internal Voltage Reference	Measure V_{REF} voltage when I_{REF}=0 and I_{REF}=20 mA.	4.85	5.00	5.15	V
V_{REF}OK Threshold	Adjust V_{REF} from 4.8V-4.0V until PWM1,2 goes low.	4.30	4.55	4.70	V
■ **Low V_{CC} Lockout**					
V_{CC} Turnon Threshold Voltage	V_{CC} increasing until I_{CC} > 3.5mA V_{5REF} I_{LOAD} = 0mA	7.00	7.25	7.50	V
V_{CC} Turnoff Threshold Voltage	V_{CC} decreasing until I_{CC} < 3.5mA V_{5REF} I_{LOAD} = 0mA	6.30	6.70	7.10	V
Hysteresis	Turnon - Turnoff	0.40	0.55	0.70	V
■ **Clock**					
Operating Frequency1	Measure frequency from $SYNC_{OUT}$.	485.0	512.0	540.0	kHz
$SYNC_{IN}$ Input Impedance	Measure input impedance.	7.00	15.00		kΩ
$SYNC_{OUT}$ Output Low Voltage	R_{LOAD} = 2kΩ to V_{5REF}		1.00	1.50	V
$SYNC_{OUT}$ Output High Voltage	R_{LOAD} = 2kΩ to Gnd	3.50	4.20		V
$SYNC_{IN}$ Detect Frequency	Verify $SYNC_{OUT}$ = $SYNC_{IN}$, R_{LOAD} = 2kΩ to Gnd	425.0		555.0	kHz
Max. Low SYNC Rej. Frequency	Verify $SYNC_{OUT}$ = FCLK when R_{LOAD} = 2kΩ to Gnd.			340.0	kHz
Min. High SYNC Rej. Frequency	Verify $SYNC_{OUT}$ = FCLK when R_{LOAD} = 2kΩ to Gnd.	690			kHz
$SYNC_{IN}$ Input Threshold Voltage	Functional Testing Verify FCLK from 1.0V to 2.8V.	0.90	1.85	2.90	V
Main PWM Clock Pulse Width	(GBD) - CLPH1 One Shot Pulse Width	80.0	100.0	120.0	ns
Aux PWM Clock Pulse Width	(GBD) -CLPH2 One Shot Pulse Width	80.0	100.0	120.0	ns
■ **Bias Supply Error Amplifier**					
Output Low Voltage	V_{SS} > 12.6V. Measure OAOUT voltage when sinking 1.0 mA.		43.0	85.0	mV
Output High Voltage	V_{SS} < 11.4V. Measure OAOUT voltage when sourcing 150μA.	4.55	4.75		V
Output High Source Current	V_{SS} < 11.4V. Measure OAOUT source current when OAOUT = 0.5V.	150.0	225.0	300.0	μA

Electrical Characteristics: T_J = -40°C to 125°C, V_{SS} = 9 to 16V, V_{5REF} I_{LOAD} = 2mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD=6V, OVSD = 0V, ENABLE = 0V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3V, R_{FADJ} = R_{DLYSET} = 27.4kΩ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Bias Supply Error Amplifier: continued					
Output Low Sink Current	V_{SS} > 12.6V. Measure OAOUT sink current when OAOUT = 2.5V.	3.0	20.0	50.0	mA
V_{SS} Set Point	Adjust V_{SS} until OAOUT goes low.	11.60	12.25	12.80	V
Large Signal Gain	(GBD)	15.00			V/mV
Unity Gain Bandwidth	(GBD)		1.00		MHz
Common Mode Input Range	(GBD)	1.00		2.00	V
■ V_{SS} Voltage					
V_{SS} Reset Voltage	Toggle ENABLE between Gnd & V_{CC}, then adjust V_{SS} from 2.0V-0.8V until OAOUT goes high.	1.00	1.40	1.80	V
■ Undervoltage Lockout					
UVSD Turn On Threshold Voltage	Adjust UVSD from 4.7V-5.3V until GATE 1, 2 goes high.	4.80	5.00	5.10	V
UVSD Turn Off Threshold Voltage	Adjust UVSD from 5.1V-4.3V until GATE 1, 2 goes low.	4.45	4.70	4.95	V
Hysteresis	Turnon - Turnoff	0.20	0.27	0.40	V
UVSD Input Bias Current	Set UVSD=0V. Measure Current out of UVSD lead.		0.20	0.50	µA
■ Overvoltage Lockout					
OVSD Threshold Voltage	Adjust OVSD from 4.7V-5.3V until GATE 1, 2 goes low.	4.85	5.00	5.15	V
OVSD Input Bias Current	Set OVSD=0V. Measure Current out of OVSD lead.		0.20	0.50	µA
■ ENABLE & PROGRAM					
ENABLE Lead Output Current	Measure current out of ENABLE when ENABLE = 0V.	100.0	266.0	500.0	µA
PROGRAM Lead Output Current	Measure current out of PROGRAM when PROGRAM = 0V.	20.0	60.0	100.0	µA
PROGRAM Threshold Voltage	ENABLE = Gnd. Adjust PROGRAM from 1.0V - 1.8V until GATE 1, 2 goes high.	1.20	1.40	1.60	V
ENABLE Threshold Voltage	PROGRAM = Gnd. Adjust ENABLE from 1.0V - 1.8V until GATE 1, 2 goes high.	1.20	1.40	1.60	V
■ Output Undervoltage Delay					
OUVDELAY Charging Current	Set OUVDELAY = 1V, V_{FB1} = 4.4V Measure OUVDELAY I_{CHARGE}.	7.50	10.00	12.50	µA
OUVDELAY Latchoff Voltage	Toggle ENABLE between Gnd & V_{CC}, then adjust OUVDELAY from 4.7V - 5.3V until GATE 1, 2, goes low.	4.80	5.00	5.20	V
OUVDELAY Set Current	OUVDELAY = VOCLO + 50mV Measure current into OUVDELAY.		0.50	1.00	mA
V_{FB1} Charge Threshold	V_{SS}=1V. Toggle ENABLE between Gnd & V_{CC}, adjust V_{FB1} from 3.8V - 4.6V until GATE 1, 2 goes low.	4.05	4.22	4.40	V
V_{FB2} Charge Threshold	V_{SS} = 1V. Toggle ENABLE between Gnd & V_{CC}, adjust V_{FB2} from 3.8V - 4.6V until GATE 1, 2 goes low.	3.90	4.15	4.35	V

Electrical Characteristics: T_J = -40°C to 125°C, V_{SS} = 9 to 16V, V_{5REF} I_{LOAD} = 2mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD=6V, OVSD = 0V, ENABLE = 0V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3V, R_{FADJ} = R_{DLYSET} = 27.4kΩ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Current Limit Circuits					
I_{LIM1} Current Limit Threshold Voltage	Adjust I_{LIM1} from 1.0V - 1.3V until GATE1 goes low.	1.16	1.24	1.30	V
I_{LIM1} Short Circuit Threshold Voltage	Adjust I_{LIM1} from 1.30V - 1.50V until GATE1 skips 2-cycles with reference to $SYNC_{OUT.}$	1.35	1.44	1.51	V
I_{LIM1} Input Bias Current	Set I_{LIM1}=0V. Measure current out of I_{LIM1} lead.		0.50	5.00	µA
I_{LIM2} Current Limit Threshold V	Adjust I_{LIM2} from 1.0V - 1.3V until GATE2 goes low.	1.16	1.24	1.30	V
I_{LIM2} Short Circuit Threshold Voltage	Adjust I_{LIM2} from 1.30V - 1.50V until GATE2 skips 2-cycles with reference to $SYNC_{OUT}$.	1.35	1.44	1.51	V
I_{LIM2} Input Bias Current	Set $I_{LIM\,2}$= 0V. Measure current out of I_{LIM2} lead.		0.50	5.00	µA
■ Voltage Feedback Control					
RAMP1 Offset Voltage	V_{FB1}=0V. Adjust RAMP1 from 0V - 0.3V until GATE1 goes low. Measure V_{RAMP1}.	0.08	0.13	0.20	V
RAMP1 Input Bias Current	Set RAMP1 = 0V. Measure Current out of RAMP1 lead.		0.50	5.00	µA
RAMP2 Offset Voltage	V_{FB2} = 0V. Adjust RAMP2 from 0V-3V until GATE2 goes low. Measure V_{RAMP2}.	0.08	0.13	0.20	V
RAMP2 Input Bias Current	Set RAMP2 = 0V. Measure Current out of RAMP2 lead.		0.50	5.00	µA
V_{FB1} Input Impedance	Measure input impedance.	60.0	120.0	220.0	kΩ
V_{FB2} Input Impedance	Measure Input impedance.	60.0	120.0	220.0	kΩ
■ Gate1,2,2B Output Voltages	**V_{SS} = 12V. V_{CC} = V_{SS} - V_{DON}**				
GATE1 Low State	PROGRAM = 0V. Measure GATE1 voltage when sinking 1mA.		0.15	0.80	V
GATE2 Low State	PROGRAM = 0V. Measure GATE2 voltage when sinking 1mA.		0.18	0.80	V
GATE2B Low State	PROGRAM = 0V. Measure GATE2B voltage when sinking 1mA.		0.18	0.80	V
GATE2B High State	Measure V_{CC} - GATE2B voltage when sourcing 1mA.		1.65	2.00	V
GATE2 High State	Measure V_{CC} - GATE2 voltage when sourcing 1mA.		1.65	2.00	V
GATE1 High State	Measure V_{CC} - GATE1 voltage when sourcing 1mA.		1.65	2.00	V
■ Propagation Delays					
I_{LIM1} Delay to Output GATE1	Measure delay from I_{LIM1} going high to GATE1 going low.		80.0	120.0	ns
I_{LIM2} Delay to Output GATE2	Measure delay from I_{LIM2} going high to GATE2 going low.		80.0	100.0	ns
RAMP1 Delay to Output GATE1	Measure delay from RAMP1 going high to GATE1 going low.		80.0	115.0	ns
RAMP2 Delay to Output GATE2	Measure delay from RAMP2 going high to GATE2 going low.		80.0	100.0	ns

Electrical Characteristics: T_J = -40°C to 125°C, V_{SS} = 9 to 16V, V_{5REF} I_{LOAD} = 2mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD=6V, OVSD = 0V, ENABLE = 0V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3V, R_{FADJ} = R_{DLYSET} = 27.4kΩ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **GATE 2, 2B Non-Overlap Delay**					
GATE2 Turn-on Delay from GATE2B	Measure delay from GATE2B going low @1.7V to GATE2 going high @1.7V.	20.0	45.0	70.0	ns
GATE2B Turn-on Delay from GATE2	Measure delay from GATE2 going low @1.7V to GATE2B going high @1.7V.	20.0	45.0	70.0	ns
■ **GATE 1, 2, 2B Rise & Fall Times**	V_{SS}=12V, V_{CC}=V_{SS}-V_{DON}				
GATE1 Rise Time	Measure GATE1 Rise Time from 90% to 10%. C_{LOAD} = 150pF.		50.0	80.0	ns
GATE1 Fall Time	Measure GATE1 Fall Time from 10% to 90%. C_{LOAD} = 150pF.		30.0	60.0	ns
GATE2 Rise Time	Measure GATE2 Rise Time from 90% to10%. C_{LOAD} = 50pF.		50.0	80.0	ns
GATE2 Fall Time	Measure GATE2 Fall Time from 10% to 90%. C_{LOAD} = 50pF.		15.0	30.0	ns
GATE2B Rise Time	Measure GATE2B Rise Time from 90% to10%. C_{LOAD} = 50pF.		50.0	80.0	ns
GATE2B Fall Time	Measure GATE2B Fall Time from 10% to 90%. C_{LOAD} = 50pF.		15.0	30.0	ns

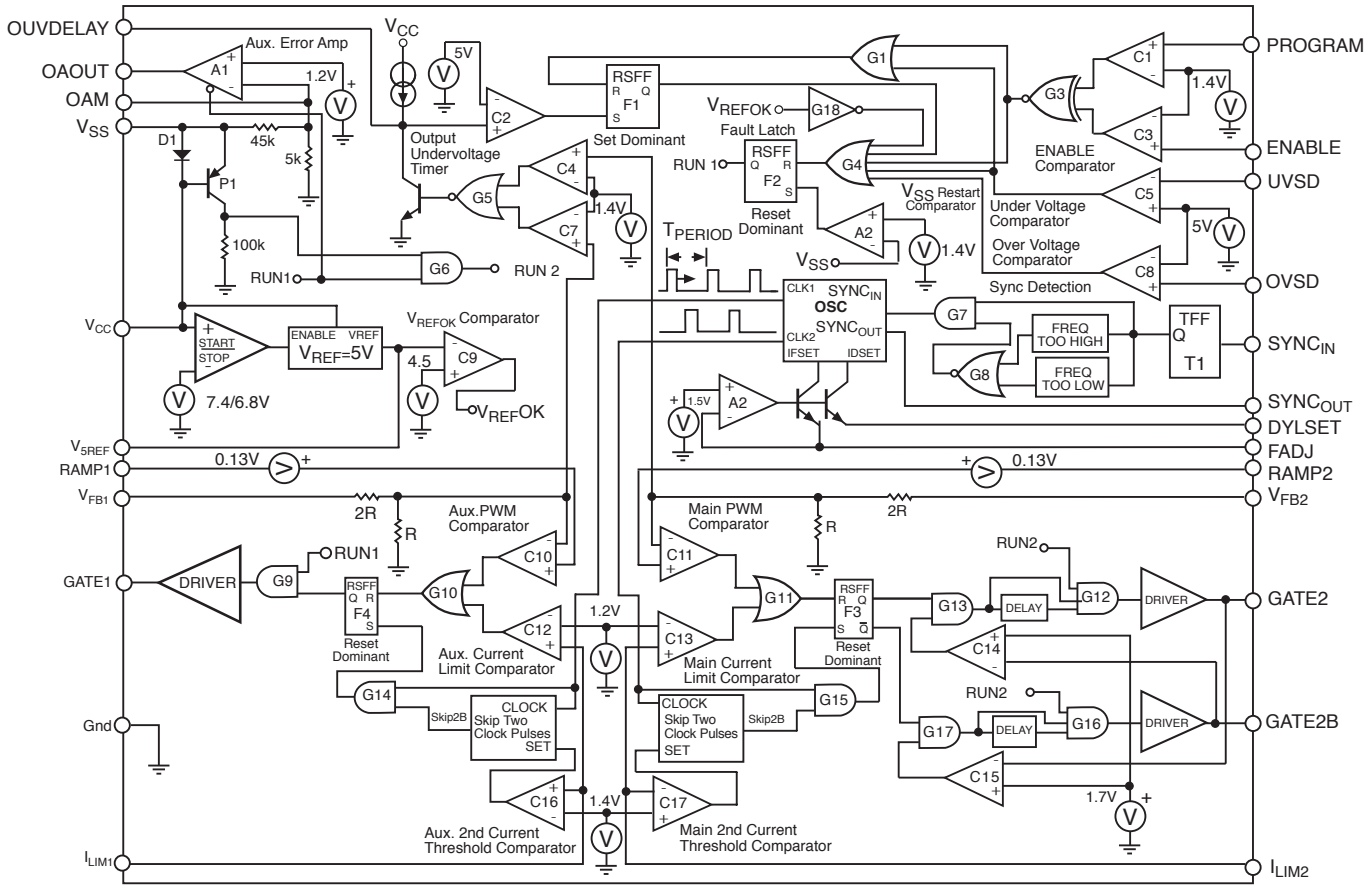
Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
1	UVSD	Undervoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage (V_{IN}) line. If the voltage on this lead is less than 5V then a fault is initiated such that GATE1, GATE2 and GATE2B go low.
2	OVSD	Overvoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage (V_{IN}) line. If the voltage on this lead exceeds 5V then a fault is initiated such that GATE1, GATE2 and GATE2B go low.
3	V_{5REF}	5V reference output lead. Capable of 20mA nominal output. If this lead falls to 4.5V, a fault is initiated such that GATE1, GATE2 and GATE2B go low.
4	OAM	Auxiliary error amplifier minus input. This lead is compared to 1.2V nominal on the auxiliary error amp plus lead and represents the V_{SS} voltage divided by ten.
5	OAOUT	Auxiliary error amplifier output lead. Source current 300μA max.
6	OUVDELAY	Output undervoltage timing capacitor lead. If the controlled output voltages of either the main or the auxiliary supply are such that either V_{FB1} or V_{FB2} is greater that 4.1V nominal, then capacitor from OUVDELAY to ground will begin charging. If the over voltage duration is such that the OUVDELAY voltage exceeds 5V, then a fault will be initiated such that GATE1, GATE2 and GATE2B will go low.
7	I_{LIM1}	Pulse by pulse over current protection lead for the auxiliary PWM. A voltage exceeding 1.2V nominal on I_{LIM1} will cause GATE1 to go low. A voltage exceeding 1.4V nominal on I_{LIM1} will cause GATE1 to go low for at least two clock cycles.
8	RAMP1	Current Ramp Input Lead for the Auxiliary PWM. A voltage which is linear with respect to current in the primary side of the auxiliary trans former is usually represented on this lead. A voltage exceeding V_{FB1} - 0.13 on RAMP1 will cause GATE1 to go low.

Package Lead Description: continued

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
9	V_{FB1}	Voltage Feedback Lead for the Auxiliary PWM. A voltage which represents the auxiliary power supply output voltage is fed to this lead. A voltage less than RAMP1+0.13 on V_{FB1} will cause GATE1 to go low.
10	V_{SS}	V_{SS} power/feedback input lead. See V_{CC} for description of power operation. In addition, this lead is fed to a divide by ten resistor divider and compared to 1.2V nominal at the positive side of the error amplifier.
11	V_{CC}	V_{CC} power input lead. This input runs off a Zener referenced supply until $V_{SS} > V_{CC}$. Then an internal diode which runs between V_{SS} and V_{CC} turns on and all main power is derived from V_{SS}.
12	GATE1	Auxiliary PWM gate drive lead. This output normally drives the FET which drives the auxiliary transformer.
13	Gnd	Ground lead.
14	GATE2	Synchronous PWM gate drive lead. This output normally drives the FET which drives the main transformer.
15	GATE2B	Synchronous PWM gate drive lead. This output normally drives the FET for the gate drive transformer used for synchronous rectification.
16	V_{FB2}	Voltage feedback lead for the synchronous PWM. A voltage which represents the main power supply output voltage is fed to this lead. A voltage less than RAMP2+0.13 on V_{FB2} will cause GATE2 to go low and GATE2B to go high.
17	RAMP2	Current ramp input lead for the synchronous PWM. A voltage which is linear with respect to current in the primary side of the main trans former is usually represented on this lead. A voltage exceeding V_{FB2} - 0.13 on RAMP2 will cause GATE2 to go low and GATE2B to go high.
18	I_{LIM2}	Pulse by pulse over current protection lead for the synchronous PWM. A voltage exceeding 1.2V nominal on I_{LIM2} will cause GATE2 to go low and GATE2B to go high. A voltage exceeding 1.4V nominal on I_{LIM2} will cause GATE2 to go low and GATE2B to go high for at least two clock cycles.
19	DLYSET	GATE2, GATE2B non-overlap time adjustment lead. A 27kΩ resistor from DLYSET to ground sets the non-overlap time to 45ns nominal.
20	FADJ	Frequency adjustment lead. A 27kΩ resistor from FADJ to ground sets the clock frequency to 512kHz nominal.
21	$SYNC_{OUT}$	Clock output lead. This is a 50% duty cycle, 1V to 5V pulse whose rising edge is in phase with GATE1. This signal can be used to synchronize other power supplies.
22	$SYNC_{IN}$	Clock synchronization lead. The internal clock frequency can be adjusted +10%, -15% by the onset of positive edges of an external clock occurring on the $SYNC_{IN}$ lead. If the external clock frequency is out side the internal clock frequency by +25%, -35% the external clock is ignored and the internal clock free runs.
23	PROGRAM	ENABLE programming input. See ENABLE for programming states. PROGRAM has at least 20μA min. of available source current.
24	ENABLE	PWM enable input. If PROGRAM is HIGH then a LOW on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If PROGRAM is LOW then a HIGH on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If ENABLE is left floating, it will pull up to a HIGH level. ENABLE has at least 100μA (min) of available source current.

Block Diagram



Theory of Application

Theory of Operation

Powering the IC

The IC has one supply, V_{CC}, and one Ground lead. If V_{SS} is used for a bootstrapped supply the diode between V_{SS} and V_{CC} is forward biased, and the IC will derive its power from V_{SS}. The internal logic monitors the supply voltage, V_{CC}. During abnormal operating conditions, all GATE drivers are held in a low state. The CS5106 requires 1.5mA nominal of startup current.

Startup

Assume the part is enabled and there are no over voltage or under voltage faults present. Also, assume that all auxiliary and main regulated output voltages start at 0V. An 8V, Zener referenced supply is typically applied to V_{CC}. When V_{CC} exceeds 7.5V, the 5V reference is enabled and the OSC begins switching. If the V_{5REF} lead is not excessively loaded such that $V_{5REF} < 4.5V$ nominal, 'V_{REF}OK' goes 'high' and 'RUN1' will go 'high', releasing GATE1 from its low state. After GATE1 is released, it begins switching according to conditions set by the auxiliary control loop and the auxiliary supply, V_{SS} begins to rise. When $V_{SS} > V_{CC} + V(D1)$, P1 turns on and 'RUN2' goes 'high', releasing GATE2 and GATE2B from their low state. GATE2 and GATE2B begin switching according to conditions set by the main control loop and the main regulated output begins to rise. See startup waveforms in Figure 1.

Soft Start

Soft start for the auxiliary power supply is accomplished by placing a capacitor between OAOUT and Ground. The error amplifier has 200μA of nominal of source current and is ideal for setting up a Soft Start condition for the auxiliary regulator. Care should be taken to make sure that the soft start timing requirements are not in conflict with any transient load requirements for the auxiliary supply as large capacitors on OAOUT will slow down the loop response. Also, the Soft start capacitor must be chosen such that during start or restart, both outputs will come into regulation before the OUVDELAY timer trips. Soft Start for the main supply is accomplished by charging soft start capacitor C6 through D5 and R7 at start up. After the main supply has come into regulation C6 continues to charge and is disconnected from the feedback loop by D8.

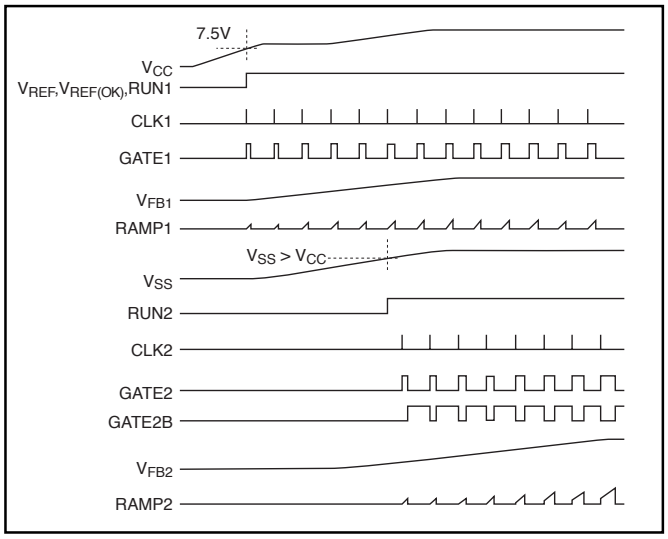


Figure 1: Startup waveforms.

Voltage and Current Ramp PWM Comparator Inputs ($V_{FB1,2}$ and RAMP1,2 leads)

C10 and C11 are the PWM comparators for the auxiliary and main supplies. The feedback voltage (V_{FB}) is divided by three and compared with a linear, voltage representation of the current in the primary side of the transformer (RAMP). When the output of the feedback comparator goes 'high', a reset signal is sent to the PWM flip-flop and the GATE driver is driven 'low'. A 130mV offset on the RAMP leads allows the drivers to go to 0% duty cycle in the presence of light loads.

Feedback Voltage for GATE1 Driver (V_{FB1})

Typically the output of the auxiliary error amplifier (A1) is tied to V_{FB1}. The V_{SS} output is programmed to 12V by a 10:1 resistive divider on the negative input of the error amplifier and a fixed 1.2V reference on the positive input of the error amplifier.

Pulse by Pulse Over Current Protection and Hiccup Mode ($I_{LIM1,2}$ leads)

C12 and C13 are the pulse by pulse current limit comparators for the auxiliary and main supplies. When the current in the primary side of the transformer increases such that the voltage across the current sense resistor exceeds 1.2V nominal, the output of the current limit comparator goes 'high' and a reset signal is sent to the PWM flip-flop and the GATE driver is driven 'low'.

C16 and C17 are the second threshold, pulse by pulse current limit comparators for the auxiliary and main supplies. If the current in the primary side of the transformer increases so quickly that the current sense voltage is not limited by C12 or C13 and the voltage across the current sense resistor exceeds 1.4V, the second threshold comparator will trip a delay circuit and force the GATE driver stage to go low and stay low for the next two clock cycles.

Undervoltage and Overvoltage Thresholds

C5 and C8 are the undervoltage and overvoltage detection comparators. Typically, these inputs are tied across the middle resistor in a three resistor divider with the top resistor to V_{IN} and bottom resistor to Ground. The under voltage comparator has 200mV of built in hysteresis with respect to a direct input on the UVSD lead. The under voltage comparator has its positive input referenced to 5V while the over voltage comparator has its negative input referenced to 5V. The output of both comparators are ORed at (G4) with the over current and enable inputs. The output of G4 feeds the input to the fault latch (F2).

PROGRAM and ENABLE Leads

The PROGRAM lead controls the polarity of the ENABLE lead. If the PROGRAM lead is 'high' or floating, the GATE outputs will go low if the ENABLE input is tied 'high' or floating. If the PROGRAM lead is tied low, the GATE outputs will go low if the ENABLE input is tied 'low'. If the part is then enabled after switching the outputs low, the part will restart according to the procedure outlined in the "Startup" section.

FAULT Logic

If a V_{REF}, UVSD or OVSD fault occurs at any time, G4 resets the fault latch (F2). RUN1 goes low and all gate drivers cease switching and return to their 'low' state. When RUN1 goes low, the output of the auxiliary op-amp (A1) discharges the soft start capacitor and holds it low while RUN1 is low. If the fault condition is removed before the OUVDELAY timer is tripped, the IC will restart the power supplies when $V_{SS} < 1.4V$. If the OUVDELAY timer trips, the power supply must be restarted as explained in the following section.

Output Undervoltage Delay Timer for the Main and Auxiliary Regulated Outputs

C7 and C4 are the output under voltage monitor comparators for the auxiliary and main supplies. If a regulated output drops such that its associated V_{FB} voltage exceeds 4.1V, the output undervoltage monitor comparator goes 'high' and the OUVDELAY capacitor begins charging from 0V. A timing relation is set up by a 10μA nominal current source, the OUVDELAY capacitor and a 5V fault threshold at the input of C2 (see Figure 2). If any regulated output drops and stays low for the entire charge time of the OUVDELAY capacitor, a fault is triggered and all GATE drivers will go into a low state.

Once this fault is triggered, the IC will restart the power supplies only if the OUVDELAY fault is reset and ENABLE or UVSD is toggled while $V_{SS} < 1.4V$. To reset the OUVDELAY fault, both the V_{FB} inputs must be less than 4.1V. In the application circuit shown, V_{FB1} is brought low by OAOUT when RUN1 stops the oscillators. V_{FB2} is brought low when V_{AUXP} bleeds down and the V_{FB2} opto-isolator is no longer powered.

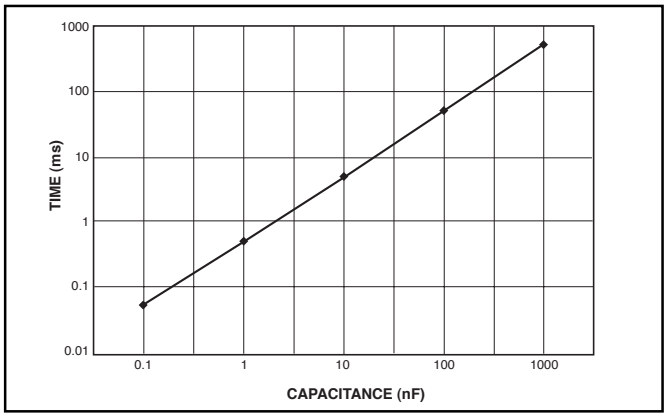


Figure 2: OUVDELAY Time vs. OUVDELAY Capacitance

Theory of Application: continued

FADJ and DLYSET Leads

Amplifier A2 and transistor N3 create a current source follower whose output is FADJ. An external resistor from FADJ to ground completes the loop. The voltage across the resistor is set by a buffered, trimmed, precision reference. In this fashion, an accurate current is created which is used to charge and discharge an internal capacitor thereby creating an oscillator with a tight frequency tolerance. For FADJ resistor value selection, see Figure 3. Transistor N2 is in parallel with N3 and is used to created an independent current across the resistor from DLYSET to ground. This current is used to program the GATE non-overlap delay blocks in the main PWM drivers. For DLYSET resistor value selection, see Figure 4.

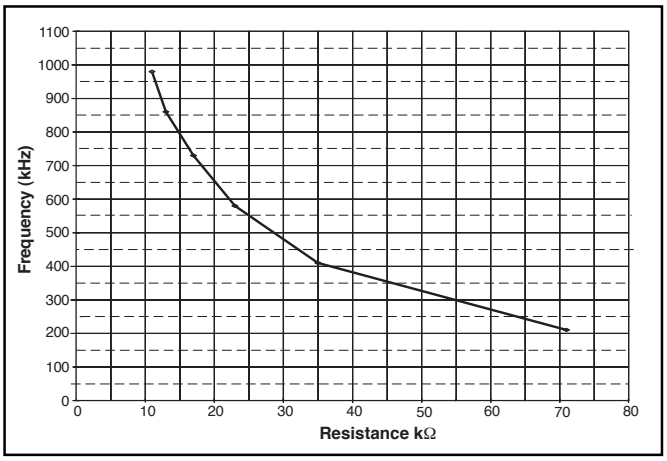


Figure 3: $SYNC_{OUT}$ Frequency vs. FADJ Resistors

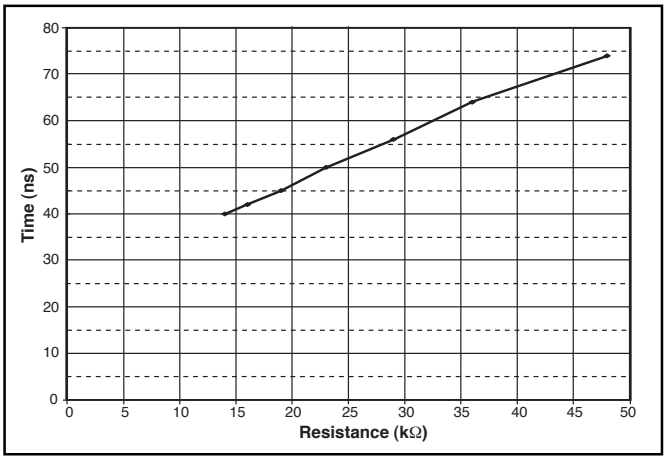


Figure 4: GATE Non-Overlap Time vs. DLYSET Resistance

Oscillator

The oscillator generates two clock signals which are 180 degrees out of phase with respect to time. One clock signal feeds the main driver and the other feeds the auxiliary driver. Because the drivers are never turned on at the same time, ground noise and supply noise is minimized. The clock signals are actually 100ns pulse spikes. These spikes create a narrow driver turn-on window. This narrow window prevents the driver from spurious turn on in the middle of a clock cycle. The oscillator can be synchronized by an external clock (slave) or drive the clocks of other controllers (master). See Figure 5 for the relationship between SYNC, CLK, and GATE waveforms.

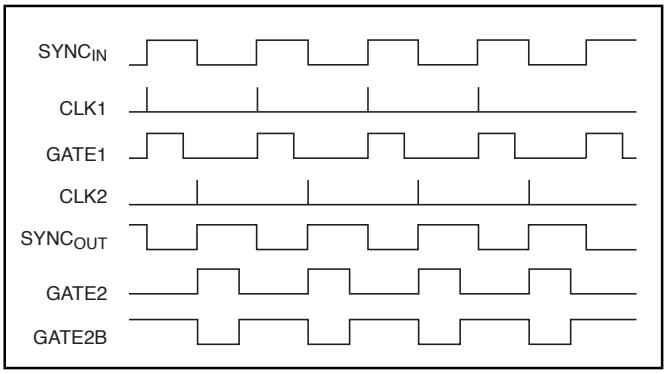


Figure 5: SYNC, GATE and CLOCK waveforms.

$SYNC_{IN}$ and $SYNC_{OUT}$ Leads

Multiple supplies can be synchronized to one supply by using the SYNC leads. The $SYNC_{IN}$ and $SYNC_{OUT}$ pulses are always 180 degrees out of phase. The $SYNC_{IN}$ input is always in phase with the clock signal for the main driver and the $SYNC_{OUT}$ output is always in phase with the clock signal for the auxiliary driver. If the IC is being used as a slave, the incoming frequency must be within +10%, -20% of the programmed frequency set by its own FADJ resistor. If the frequency on the $SYNC_{IN}$ lead is outside the internal frequency by +25%, -35%, the $SYNC_{IN}$ input will be ignored. If the SYNC signal stops while the power supplies are in synchronized operation, the synchronized supplies will stop and restart free running. If the $SYNC_{IN}$ signal drifts out of frequency specification while the power supplies are in synchronized operation, the synchronized supplies will begin to free run without restarting.

Slope Compensation

DC-DC converters with current mode control require slope compensation to avoid instability at duty cycles greater than 50%. A slope is added to the current sense waveform (or subtracted from the voltage waveform) that is equal to a percentage (75% typical) of the down slope of the inductor current. In the application diagram shown, the bootstrap (flyback) transformer inductance can be chosen so that the duty cycle never exceeds 50% and therefore does not require slope compensation. The buck indicator in the forward converter would typically be chosen to work in continuous conduction mode with a maximum duty cycle of 50-60% and would require slope compensation. Slope compensation is accomplished as follows: R9 and C9 form a ramp waveform rising each time GATE 2 turns on. C9 is discharged through D3 to the same level each cycle regardless of duty cycle. R10 and R11 are chosen to control the amount of slope compensation. C10 provides filtering for noise and turn-on spikes. To calculate the required slope compensation, calculate the buck indicator down current and the corresponding voltage slope at the current sense resistor - R12.

The buck inductor down slope is:

$$\text{Inductor_Slope} = \frac{V_{OUT} + V_{Q5}}{L1(\mu H)}\left(\frac{A}{\mu s}\right)$$

The equivalent down slope at the current sense resistor for this application circuit is:

$$\text{Slope @ R12} = \text{Inductor_Slope} \times \frac{NS_{T2}}{NP_{T2}} \times \frac{NP_{T3}}{NS_{T3}} \times R12\left(\frac{V}{\mu s}\right)$$

After choosing R9 and C9 to generate a ramp with a time constant of about 5 times the oscillator period, R10 and R11 can be chosen for the voltage at RAMP2 to be 1.75 of the voltage across R12.

Synchronous Rectification

Synchronous rectification was chosen to reduce losses in the forward converter. Improvements in efficiency will be most significant in low voltage, medium and high current converters where improvement in conduction loss offsets any added losses for gate drive.

In the application circuit Q4 is turned on and off by the forward transformer. Q5 is turned on and off through pulse transformer T4 and the gate driver formed by Q6 and Q7. Because Q4 and Q5 are driven through different types of components, differences in propagation delay must be considered. The DLYSET resistor should be chosen to avoid shoot-through or excessive off time.

Gate Drive Capability

All GATE drive outputs have nominal peak currents of 0.5A. See Figures 6 and 7 for typical rise and fall times.

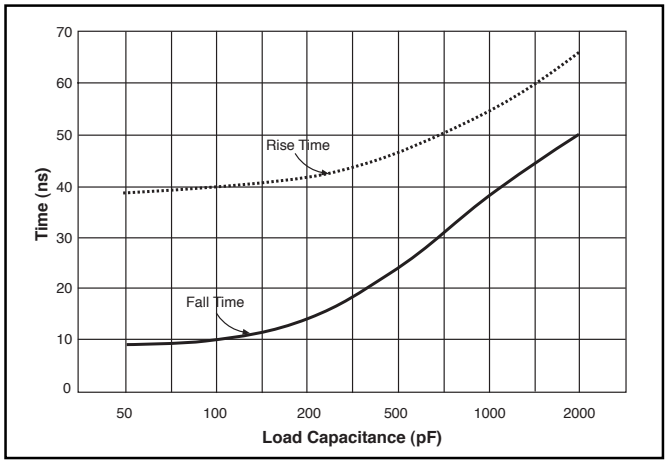


Figure 6: Typical GATE2, 2B switching times.

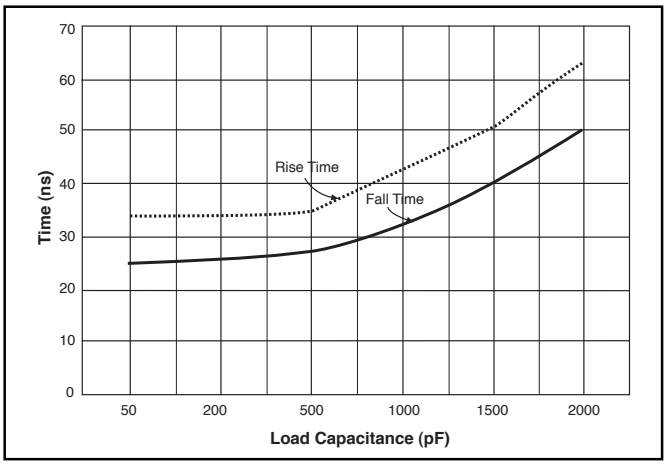


Figure 7: Typical GATE1 switching times.

Design Considerations

The circuit board should utilize high frequency layout techniques to avoid pulse width jitter and false triggering of high impedance inputs. Ground plane(s) should be employed. Signal grounds and power grounds should be run separately. Portions of the circuit with high slew rates or current pulses should be segregated from sensitive areas. Shields and decoupling capacitors should be used as required.

Special care should be taken to prevent coupling between the SYNC leads and the surrounding leads. Depending on the circuit board layout and component values, decoupling capacitors or reduction in resistor values might be required to reduce noise pick-up on the FADJ and DLYSET resistors. Decoupling capacitors or active pull-up/down might be required to prevent false triggering of the ENABLE and PROGRAM leads.

Package Specification

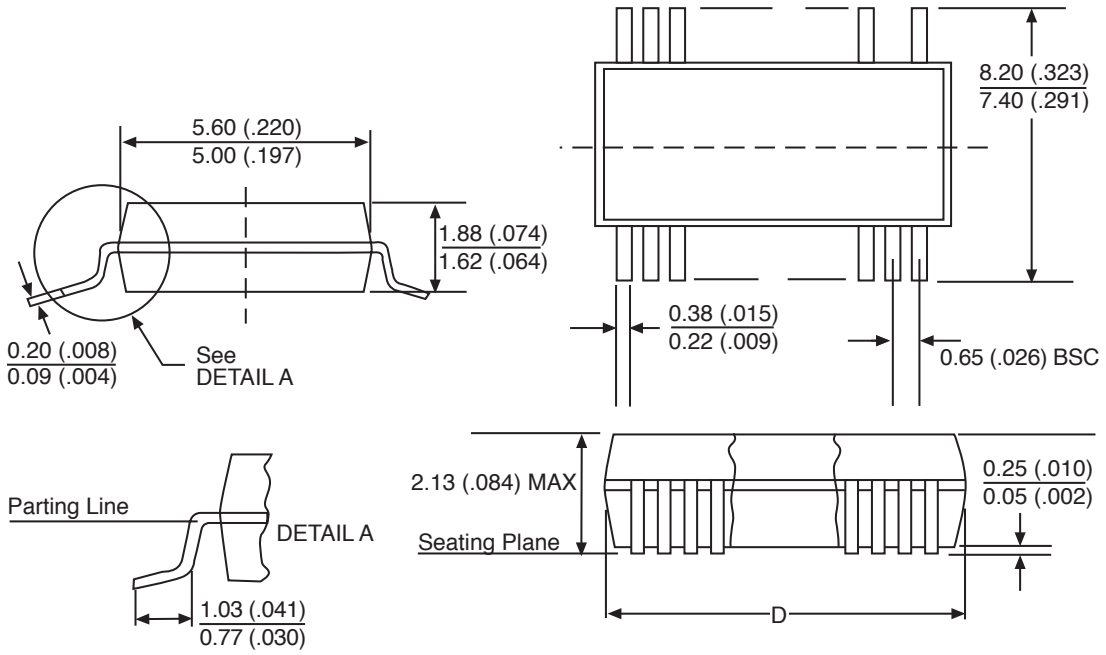
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
24 Lead SSOP	8.50	7.90	.335	.311

PACKAGE THERMAL DATA

Thermal Data		24 Lead SSOP	
$R_{\Theta JC}$	typ	23	°C/W
$R_{\Theta JA}$	typ	117	°C/W

SSOP (SW); 5.3mm Body



REF: JEDEC MO-150

Ordering Information

Part Number	Description
CS5106LSW24	24 Lead SSOP
CS5106LSWR24	24 Lead SSOP *(tape & reel)*

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